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First Named Inventor	Akram et al.
Art Unit	2822
Examiner Name	D. Graybill
Attorney Docket Number	2269-3846.2US (98-0796.02/US)

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ CD, Number of CD(s) ____
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- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Brief (12 pages); Claims Appendix (5 pages); Evidence Appendix (4 pages)
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

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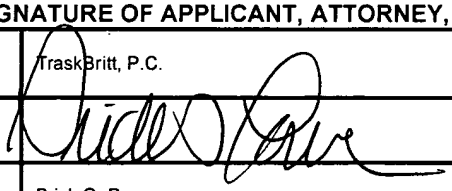
Signature			
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Akram et al.

Serial No.: 09/832,160

Filed: April 9, 2001

For: WAFER-LEVEL PACKAGE AND METHODS OF FABRICATING

Confirmation No.: 8501

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Group Art Unit: 2822

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APPEAL BRIEF

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Sirs:

This Appeal Brief is being filed in compliance with the requirements of 37 C.F.R. § 41.37(c)(1) and with the fee required by 37 C.F.R. § 41.20(b)(2).

(1) REAL PARTY IN INTEREST

U.S. Application Serial No. 09/832,860 (hereinafter "the '860 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 010090, Frame No. 0621. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellants nor the undersigned attorney are aware of any action pending before the Board of Patent Appeals and Interferences (hereinafter "the Board") that would affect or influence the Board's decision in the above-referenced appeal.

(3) STATUS OF CLAIMS

The above-referenced application was filed with thirty-four (34) claims. Claims 10 and 11 were canceled without prejudice or disclaimer. No new claim has been added.

Claims 4, 9, and 23-34 have been withdrawn from consideration.

Claims 1-3, 5-8, and 12-22, which have been considered, are subject to final rejections, which are to be reviewed in the above-referenced appeal.

(4) STATUS OF AMENDMENTS

The most recent Amendment that included claim revisions was mailed on February 21 2006. That Amendment was accompanied by explanations as to the patentability of

the claims, which were again rejected in a final Office Action dated May 22, 2006. Further reasoning as to the patentability of claims 1-9 and 12-34 was presented in a Response to Final Office Action dated August 22, 2006. This reasoning was also rejected, as evidenced by an Advisory Action dated September 15, 2006.

In view of the Examiner's continued reluctance to allow claims 1-9 and 12-34, a Notice of Appeal was filed on September 22, 2006. This Appeal Brief is being submitted within two months of the date on which the Notice of Appeal was mailed.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

While reference characters are used in the following summary to identify examples of claim elements that are shown in the drawings, it is noted that the reference characters are included merely to ensure full compliance with the requirements of 37 C.F.R. § 41.37(c)(1)(v), and that their inclusion merely points to examples in the as-filed disclosure that do not limit the scope of independent claim 1 or any other claim that remains pending in the above-referenced application. Rather, the scope of each claim is limited only by the plain language thereof, and includes the full scope of available equivalents to each recited element.

Independent claim 1 is drawn to a method for fabricating a chip-scale package. The method of independent claim 1 includes positioning a preformed polymeric film 18 over a semiconductor device 12. *See, e.g.,* paragraphs **[0014]**, **[0050]**, **[0055]**; FIGs. 2, 2A, 2B. As the polymeric film 18 is positioned over the semiconductor device 12, at least one aperture 20 that has already been formed therein is substantially aligned with a corresponding bond pad 16 of the semiconductor device 12. *See, e.g.,* paragraphs **[0015]**, **[0057]**; FIG. 3.

In the method of independent claim 1, conductive material 121 is also introduced into at least one aperture 120 of a preformed polymeric film 118. *See, e.g.,* paragraph **[0016]**; FIG. 4B. Specifically, conductive material 121 that is in an at least partially liquid state is introduced into the at least one aperture 120. *See, e.g.,* paragraphs **[0062]**, **[0063]**; FIG. 4B.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 103(a) rejections of claims 1-3, 5-8, 12, 13, 15-17, 19, and 20 for being drawn to subject matter that is allegedly unpatentable over the subject matter taught in U.S. Patent 5,946,555 to Crumly et al. (hereinafter "Crumly"), in view of teachings from U.S. Patent 6,071,810 to Wada et al. (hereinafter "Wada");

(B) The rejections of claims 1-3, 5-8, and 12-22 under 35 U.S.C. § 103(a) for reciting subject matter that is purportedly obvious in view of teachings from U.S. Patent 6,284,563 to Fjelstad (hereinafter "Fjelstad"), in view of the subject matter taught in Crumly and Wada;

(C) The rejections of claims 14, 18, 21, and 22 under 35 U.S.C. § 103(a) for being directed to subject matter which is assertedly unpatentable over the teachings of Crumly, Wada, and Fjelstad; and

(D) The 35 U.S.C. § 103(a) rejections of claims 21 and 22 under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the teachings of Crumly and Wada, in view of teachings from U.S. Patent 6,294,407 to Jacobs (hereinafter "Jacobs") or over the teachings of Crumly, Wada, Fjelstad, and Jacobs.

(7) ARGUMENT

(A) REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1-3, 5-8, and 10-22 stand rejected under 35 U.S.C. § 103(a).

(1) APPLICABLE LAW

The standard for establishing, maintaining, and upholding a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(2) ART RELIED UPON

Crumly

Crumly teaches a process in which a preformed element, which Crumly refers to as a "substrate decal 16," that comprises a flexible polyimide film or a circuit board, is positioned over a semiconductor device 12. FIG. 1. The substrate decal 16 of Crumly includes apertures 27 that are aligned with corresponding bond pads 14 of the semiconductor device 12 as the substrate decal 16 is positioned over the semiconductor device 12. FIG. 1. Once the substrate decal 16 has been positioned over and adhered to the semiconductor device 12 with adhesive 24 (FIG. 2),

conductive material 32 is introduced into the apertures 27 of the substrate decal 16 and in contact with the bond pads 14 of the semiconductor device 12 (FIG. 3). Crumly indicates that sputtering or electrolytic deposition processes may be used to introduce conductive material into the apertures 27. Col. 2, lines 9-23.

Wada

The teachings of Wada relate to the introduction of conductive material into grooves and apertures in silicon dioxide films. Wada teaches, among other things, that an Al-Sn alloy may be deposited into the grooves and apertures by sputtering, and that the Al-Sn within the grooves and apertures may be heated to a liquid phase. The Al-Sn is not heated until after it is present within the grooves and apertures, either following deposition (col. 102, lines 8-10) or during deposition so that the Al-Sn becomes liquefied once it is deposited on the silicon dioxide film (col. 102, lines 10-14).

Fjelstad

The disclosure of Fjelstad relates to, among a variety of other things, placing polymeric sheets on and adhering them to semiconductor devices 100 to form passivation layers 130 over the semiconductor devices 100. Col. 8, lines 39-41. Once a passivation layer 130 has been applied to a semiconductor device 100, a registering system is used to locate contacts 110 of the semiconductor device. Col. 8, lines 41-43. Thereafter, removal processes are used to "selectively remove the passivation layer **130** above the contacts **110**." Col. 8, lines 46-49. Conductive material 150 is then plated onto the exposed contacts 110. Col. 9, lines 24-62.

(3) ANALYSIS

(a) CRUMLY IN VIEW OF WADA

Claims 1-3, 5-8, 12, 13, 15-17, 19, and 20 have been rejected for being drawn to subject matter that is allegedly unpatentable over the subject matter taught in Crumly, in view of teachings from Wada.

It is respectfully submitted that there are several reasons that teachings from Crumly and Wada do not support a *prima facie* case of obviousness against any of claims 1-3, 5-8, 12, 13, 15-17, 19, of 20.

First, it is respectfully submitted that Crumly and Wada do not teach or suggest each and every element of any of claims 1-3, 5-8, 12, 13, 15-17, 19, or 20. With respect to the subject matter to which independent claim 1 is drawn, it is respectfully submitted that neither Crumly nor Wada, taken either separately or together, teaches or suggests "introducing conductive material in an at least partially liquid state into at least one aperture." The Examiner has already noted, at page 4 of the final Office Action, that, because the disclosure of Crumly is limited to use of sputtering or electrolytic deposition processes to introduce conductive material into apertures, "Crumly does not appear to . . . disclose introducing the conductive material in an at least partially liquid state." The teachings of Wada are likewise limited to sputtering conductive materials to deposit the conductive materials within grooves or apertures of a silicon dioxide film. *See, e.g.,* col. 102, lines 8-14. Wada teaches that the conductive materials are not liquefied until after they are present within the grooves or apertures. *See, e.g., id.*

Second, it is respectfully submitted that, without the benefit of hindsight that the pending claims of the '160 Application provide, one of ordinary skill in the art wouldn't have had any motivation to combine teachings from Crumly and Wada in the asserted manner. This is particularly true when the teachings or Crumly and Wada are considered in their entireties. Specifically, the teachings of Crumly relate to the use of polyimide decals. As those of ordinary skill in the art are aware, polyimides are stable of temperatures of about 300° C. to about 400° C. *See* Lau, John H., CHIP ON BOARD TECHNOLOGIES FOR MULTICHIP MODULES, page 232 (Van Nostrand Reinhold, 1994) (hereinafter "Lau"), a copy of which is enclosed in the EVIDENCE APPENDIX to this Appeal Brief. Wada teaches, however, that a substrate upon which an Al-Sn alloy is deposited is "heated to a temperature of 420° C. or more . . . to obtain a liquid phase of the Al-Sn alloy." Col. 91, lines 37-40. While silicon dioxide films can withstand such high temperatures, it is respectfully submitted that, without the benefit of hindsight that the claims of the '160 Application provide, one of ordinary skill in the art wouldn't have been motivated to heat a polyimide film to such a high temperature.

Third, as one of ordinary skill in the art wouldn't have any reason to expect that the polyimide decal of Crumly could withstand the high temperature of the process disclosed in Wada, it is respectfully submitted that one of ordinary skill in the art would have had no reason to expect that teachings from Crumly and Wada could be successfully combined in the asserted manner.

Therefore, a *prima facie* case of obviousness has not been established against the subject matter recited in independent claim 1. As such, it is respectfully submitted that, under

35 U.S.C. § 103(a), the subject matter to which independent claim 1 is drawn is allowable over teachings from Crumly and Wada, taken either together or separately.

Each of claims 2, 3, 5-8, 12, 13, 15-17, 19, and 20 is allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

(b) FJELSTAD, CRUMLY, AND WADA

Claims 1-3, 5-8, and 12-22 are rejected for reciting subject matter that is purportedly obvious in view of teachings from Fjelstad, in view of the subject matter taught in Crumly and Wada.

Like Crumly and Wada, Fjelstad includes no teaching or suggestion of "introducing conductive material in an at least partially liquid state into . . . at least one aperture," as required of the method of independent claim 1. Furthermore, Fjelstad does not overcome the aforementioned deficiencies in the asserted combination of teachings from Crumly and Wada. Therefore, teachings from Fjelstad, Crumly, and Wada do not support a *prima facie* case of obviousness against any of claims 1-3, 5-7, or 12-22, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

(c) CRUMLY, WADA, AND FJELSTAD

Claims 14, 18, 21, and 22 also stand rejected for being directed to subject matter which is assertedly unpatentable over the teachings of Crumly, Wada, and Fjelstad.

Each of claims 14, 18, 21, and 22 is allowable, among other reasons, for depending indirectly from independent claim 1, which is allowable.

These claims are further allowable since one of ordinary skill in the art wouldn't have been motivated to combine teachings from these references in the asserted manner or any reason to expect that the references teachings could be successfully combined in such a way as to arrive at the inventions to which claims 14, 18, 21, and 22 are directed.

(d) CRUMLY, WADA, (FJELSTAD,) AND JACOBS

Claims 21 and 22 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the teachings of Crumly and Wada, in view of teachings from Jacobs, or over the teachings of Crumly, Wada, Fjelstad, and Jacobs.

Claims 21 and 22 are both allowable, among other reasons, for depending indirectly from independent claim 1, which is allowable.

Reversal of the 35 U.S.C. § 103(a) rejections of claims 1-3, 5-8, and 10-22 is respectfully solicited, as is the allowance of each of these claims.

(B) ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claim 1 remains generic to all of the species of invention of the second group that was identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 4, 9, and 23-34, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

(8) CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

(9) EVIDENCE APPENDIX

A copy of Lau, John H., CHIP ON BOARD TECHNOLOGIES FOR MULTICHIP MODULES, page 232 (Van Nostrand Reinhold, 1994) is included in the EVIDENCE APPENDIX as a matter of courtesy and for the sake of convenience.

(10) RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a RELATED PROCEEDINGS APPENDIX.

(11) CONCLUSION

It is respectfully submitted that:

(A) Claims 1-3, 5-8, 12, 13, 15-17, 19, and 20 are drawn to subject matter that, under 35 U.S.C. § 103(a), is patentable over the subject matter taught in Crumly, in view of teachings from Wada;

(B) The subject matter recited in each of claims 1-3, 5-8, and 12-22 is not obvious in view of teachings from Fjelstad, in view of the subject matter taught in Crumly and Wada and, thus, is allowable under 35 U.S.C. § 103(a);

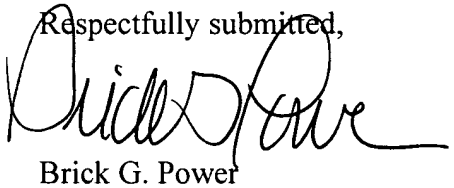
(C) Claims 14, 18, 21, and 22 are drawn to subject matter that is allowable over the teachings of Crumly, Wada, and Fjelstad and, thus, patentable under 35 U.S.C. § 103(a); and

(D) Claims 21 and 22 are under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over the teachings of Crumly and Wada, in view of teachings from Jacobs, or which is patentable over the teachings of Crumly, Wada, Fjelstad, and Jacobs.

It is further submitted that claims 4, 9, and 23-34 should be returned to consideration and allowed.

Accordingly, reversal of the final rejections of claims 1-3, 5-8, and 10-22 is respectfully requested, as is the allowance of each of claims 1-9 and 12-34.

Respectfully submitted,



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CLAIMS APPENDIX

1. A method for fabricating a chip-scale package, comprising:

positioning a preformed polymeric film including at least one aperture that extends substantially longitudinally therethrough over a semiconductor device with the at least one aperture in substantial alignment with a corresponding bond pad of the semiconductor device; and

introducing conductive material in an at least partially liquid state into the at least one aperture.

2. The method of claim 1, further comprising adhering the preformed polymeric film to the semiconductor device.

3. The method of claim 1, further comprising defining at least another aperture through the preformed polymeric film.

4. The method of claim 3, wherein defining is effected after positioning.

5. The method of claim 3, wherein defining is effected before positioning.

6. The method of claim 1, wherein introducing comprises bonding the conductive material to the corresponding bond pad.

7. The method of claim 1, further comprising depositing conductive material onto the preformed polymeric film and within the at least one aperture.

8. The method of claim 7, wherein depositing comprises chemical vapor depositing or physical vapor depositing the conductive material.

9. The method of claim 1, wherein introducing comprises placing a preformed conductive structure within the at least one aperture.

12. The method of claim 1, further comprising forming at least one contact at an end of the conductive material, opposite the semiconductor device.

13. The method of claim 12, further comprising placing a conductive structure adjacent the at least one contact.

14. The method of claim 13, wherein placing comprises applying solder to the at least one contact.

15. The method of claim 1, further comprising positioning at least one conductive trace on the preformed polymeric film and in communication with the conductive material.

16. The method of claim 15, further comprising forming at least one contact in communication with the conductive trace.

17. The method of claim 16, further comprising placing a conductive structure adjacent the at least one contact.

18. The method of claim 17, wherein placing comprises applying solder to the at least one contact.

19. The method of claim 1, further comprising placing the preformed polymeric film on at least a portion of a peripheral edge of the semiconductor device.

20. The method of claim 17, further comprising placing polymeric material at least laterally adjacent the conductive structure.

21. The method of claim 17, further comprising placing a conductive elastomer over at least one conductive structure.

22. The method of claim 21, further comprising placing another conductive structure in contact with the conductive elastomer, opposite the at least one conductive structure.

23. A method for fabricating a chip-scale package, comprising:

placing photoimageable polymeric material on a surface of a semiconductor device;

forming a polymeric film from the photoimageable polymeric material with at least one aperture extending substantially longitudinally through the polymeric film, the at least one aperture aligned with a corresponding bond pad of the semiconductor device; and introducing conductive material into the at least one aperture.

24. The method of claim 23, wherein forming comprises selectively exposing regions of the photoimageable polymeric material to electromagnetic radiation.

25. The method of claim 23, further comprising defining the at least one aperture through the polymeric film.

26. The method of claim 25, wherein defining is effected after the forming.

27. The method of claim 25, wherein defining is effected substantially simultaneously with the forming.

28. The method of claim 23, further comprising placing at least one conductive trace on the polymeric film and in communication with the conductive material.

29. The method of claim 28, further comprising placing at least one contact in communication with the at least one conductive trace.

30. The method of claim 29, further comprising placing at least one conductive structure adjacent the at least one contact.

31. The method of claim 30, further comprising placing polymeric material at least laterally adjacent the at least one conductive structure.

32. The method of claim 30, further comprising placing a conductive elastomer over the at least one conductive structure.

33. The method of claim 32, further comprising placing at least one other conductive structure in contact with the conductive elastomer, opposite the at least one conductive structure.

34. The method of claim 23, wherein forming comprises forming the polymeric film so as to extend at least partially over a peripheral edge of the semiconductor device.

EVIDENCE APPENDIX

CHIP ON BOARD TECHNOLOGIES FOR MULTICHIP MODULES

Edited by John H. Lau

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reactions – sometimes in the gas phase, but preferably on the surface – produce deposits on the wafer. The result is a high quality film deposited at a relatively low temperature.[10] As a passivator, PECVD silicon nitride is in compression.[15] Excessive thickness of the nitride has been known to cause high tensile stress in aluminum thin film lines and subsequent creep-induced voiding and failure.[18] Therefore nitride is kept thin, or modulated with an underlayer of SiO_2.

5.3.2 Polymers

Among polymeric materials, polyimides are the popular choice for chip passivation. They are stable at temperatures of 300 to 400°C, making them compatible with chip joining even with high lead solders. Film thickness and properties are readily controllable by the formulation and process parameters. A major advantage over inorganic passivations is the ability of polyimide to absorb thin film stresses imparted from the deposition of interconnection metallization and solder,[13] and from subsequent thermal exposures. This arises from its low elastic modulus and rapid stress relaxation, even at low temperatures.[19] Also, polyimides generally have a lower dielectric constant even than sputtered SiO_2. On the negative side, polyimides are more permeable to water and ionic contaminants, and may require adhesion promoters to insure adequate adhesion to the underlying organic or inorganic insulator.

Polyimide coatings are formed by spin coating a mixture of diamine and dianhydride monomers in a solvent, usually N-methyl-pyrrolidine 2 (NMP). For a fixed formulation, the thickness is directly related to the speed of rotation. The monomers combine at low temperatures to form polyamic acid, which, like its constituents, is soluble in NMP. The film is dried at about 100°C to remove most of the solvent, thence to 250-400°C to complete solvent removal and the conversion to polyimide. The commonly used pyromellitic dianhydride-oxydianiline (PMDA-ODA) family of polyimides are isotropic in behavior. New candidates, however, such as the long polymer chain biphenyldiaminine-phenyldiamine (BPDA-PDA) polyimides tend to be anisotropic in mechanical and electrical properties.[10]

5.4 TERMINAL METALS AND SOLDERS–MATERIALS

Following chip passivation, holes are etched with a photoresist mask, thus preparing the chip for terminal metals and solder. This section discusses the various material options available for the interconnection. Section 5.5 then describes the deposition processes currently in use.